Amendments to the Specification:

Please amend the specification as follows:

Page 1, before the 1st paragraph insert the following:

This application is a continuation of application Serial No. 10/359,190, filed February 6, 2003, which is in turn a divisional of application Serial No. 10/093,935, filed on March 11, 2002, which is in turn a continuation of application Serial No. 09/916,578, filed on July 30, 2001, now U.S. Patent No. 6,373,785, which is in turn a continuation of application Serial No. 09/812,820, filed on March 21, 2001, now U.S. Patent No. 6,317,382, which is in turn a divisional of application Serial No. 09/433,338, filed November 4, 1999, now U.S. Patent No. 6,249,481, which in turn is a divisional of application Serial No. 09/236,832, filed January 25, 1999, now U.S. Patent No. 5,995,442, which is in turn a divisional of application Serial No. 09/017,948, filed February 3, 1998, now U.S. Patent No. 5,926,436, which is in turn a continuation of application Serial No. 08/779,902, filed January 7, 1997, now U.S. Patent No. 5,740,122, which is in turn a continuation of application Serial No. 08/463,394, filed June 5, 1995, now U.S. Patent No. 5,612,925, which is a continuation of application Serial No. 08/223,222, filed April 5, 1994, now U.S. Patent No. 5,500,829, which is in turn a divisional of application Serial No. 07/775,602, filed October 15, 1991, now U.S. Patent No. 5,313,437, which claims priority from Japanese Patent Application 2-273170, filed October 15, 1990 and Japanese Patent Application 3-255354, filed October 2, 1991. The entire contents of each of the aforementioned applications are incorporated by reference herein.

Please replace paragraph starting at page 3, line 9 through page 6, line 25 with the following rewritten paragraph:

~~SUMMARY OF THE INVENTION~~

~~An object of the present invention is to provide, with due consideration to the drawbacks of such conventional devices, a semiconductor memory device provided with an easily-controllable dynamic memory which can be accessed at high speed.~~

~~Access by the semiconductor device of the present invention commences with an internal operation synchronized with a basic clock signal which is input at an almost continuous, fixed frequency. After the address is obtained, the operation which determines "read-out" or "write-in", begins after a certain cycle number of fixed cycles which are basic clock cycles, input at an almost fixed frequency. The operation is controlled by a specifying signal for specifying a cycle which acts as the starting point for counting these cycles.~~

~~A first type semiconductor memory device according to the first embodiment of the present Invention, comprises:~~

~~a memory cell group comprising a plurality of memory cells arranged in matrix;~~

~~specification means for specifying sequentially memory cells addressed by consecutive addresses in the memory cells, and for entering them in an active state;~~

~~data input/output (I/O) means for performing a data read-out/write-in operation (data I/O operation) for the consecutive memory cells specified by the specification means under a control based on a read-out/write-in signal provided from an external section;~~

~~count means for counting the number of cycles of a basic clock signal provided from an external section; and~~

~~control means for receiving at least one or more specification signals provided from an external section,~~

~~for outputting a control signal per specification signal for specifying a particular cycle as a starting cycle to count the number of the cycles of the basic clock signal, and~~

~~for instructing the count means to count the number of counts of the basic clock signal based on the control signal, and for controlling a specification operation executed by the specification means and the data I/O operation of the data I/O means, so that the memory access operations for the memory cell group are controlled.~~

~~A second type semiconductor memory device according to the second embodiment of the present invention, comprises:~~

~~a memory cell group comprising a plurality of memory cells grouped Into a plurality of cell blocks arranged in matrix;~~

~~selection means for outputting a selection signal provided based on a basic clock signal provided consecutively from an external section and an address signal for specifying an address of the cell block in order to select and activate the cell block by interleaving consecutively the memory cell blocks;~~

~~specification means for specifying sequentially and activating the memory cells addressed by consecutive addresses in the memory cell block in accordance with the address signal and the selection signal for activating and entering the cell block in an active state by the selection means;~~

~~data input/output (I/O) means for performing a data read-out/write-In operation (data I/O operation) for the consecutive memory cells specified by the specification means under a control based on a read-out/write-In signal provided from an external section;~~

~~count means for counting the number of cycles of the basic clock signal provided from an external section; and~~

~~control means for receiving at least one or more specification signals provided from an external section,~~

~~for outputting a control signal per specification signal for specifying a particular cycle as a starting cycle to count the number of the cycles of the basic clock signal, and~~

~~for instructing the count means to count the number of counts of the basic clock signal based on the control signal, and for controlling a selection and activation operation executed by the selection means, a specification operation executed by the specification means and the data I/O operation executed by the data I/O means, so that by which the memory access operations for the memory cell group are controlled.~~

~~A third type semiconductor memory device according to the third embodiment of the present invention, comprises:~~

~~a memory cell group comprising a plurality of memory cells arranged in matrix;~~

~~specification means for specifying and activating at once a fixed number of the memory cells, as a package memory cell, addressed by consecutive addresses in the memory cells in accordance with a basic clock signal and an address signal provided from an external section;~~

~~store means for storing temporarily data from or to the fixed number of the memory cells specified at once by the specification means;~~

~~control means for carrying at once a data transfer operation between the fixed number of the memory cells specified at once by the specification means and the store means in accordance with the basic clock signal and the specification signal;~~

~~data input/output (I/O) means for executing sequentially a data read-out/write-in operation (data I/O operation) for the store means in accordance with the basic clock signal; and~~

~~count means for counting the number of cycles of a basic clock signal,~~

~~wherein the control means receives at least one or more specification signals provided from an external section,~~

~~outputs a control signal per specification signal for specifying a particular cycle as a starting cycle to count the number of the cycles of the basic clock signal,~~

~~instructs the count means to count the number of counts of the basic clock signal based on the control signal,~~

~~controls a specification operation executed by the specification means and the data I/O operation of the data I/O means based on the number of the cycles including the number of the cycles at least two or more counted from the particular cycle by the count means, and~~

~~so that the control means controls the memory access operations for the memory cell group.~~

~~These and other objects, features and advantages of the present invention will be more apparent from the following description of preferred embodiments, taken In conjunction with the accompanying drawings~~

SUMMARY OF THE INVENTION

According to an aspect of the present invention, there is provided a method of accessing a semiconductor device that operates in synchronism with a clock signal, comprising fetching information indicating a memory cell location in a memory cell array in synchronism with the clock signal, determining first data of a plurality of data to be transferred sequentially, decoding the information indicating the memory cell location in the memory cell array and designating the memory cell, receiving data stored in the memory cell designated by the information indicating the memory cell location in the memory cell array in synchronism with the clock signal after a predetermined number of cycles of the clock signal, and outputting a plurality of data stored in the memory cells in synchronism with the clock signal and storing a plurality of input data in the memory cells in synchronism with the clock signal.